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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,403	08/28/2003	Hugo Cheung	TI-32740.1	6534

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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,403	CHEUNG, HUGO	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The claim for priority should be updated to indicate the status of the parent application (i.e. to include the patent number and the issue date).

Specification

2. The abstract of the disclosure is objected to because it exceeds 150 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

3. Claims 17-19 are objected to because of the following informalities:

Claim 17 recites the limitation "said transmit buffering step" in line 2

Claim 18 recites the limitation "said transmit and receive shifting step" in line 2

Claim 19 recites the limitation "said receive buffering step" in line 2

There is insufficient antecedent basis for the limitations in the respective claims. It appears that applicant meant to recite "sequence" instead of "step" in the respective claims.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for "receiving and storing the new data in a receive shift register in a location of said buffer designated by **a shift pointer**" [page 12, ll. 12-20; FIG. 4], **does not** reasonably provide enablement for "receiving and storing the new data in a receive shift register in a location of said buffer designated by **a read pointer**". The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

Page 12, ll. 14-16 discloses "The RdPtr pointer comprises the location of the FIFO buffer 400 that the CPU will read from during data transmission, and is configured to increment after the CPU reads from the SPI data register" while page 16, ll. 7-10 discloses "a new byte of data can be suitably received and stored in the receive shift register 304, i.e., stored in the location of FIFO buffer 400 designated by the RdPtr pointer". It appears that the disclosure on page 16, ll. 7-10 contradicts the disclosure on page 12, ll. 14-16, FIG. 4, and the context of the invention. Furthermore, the disclosure only provides support for the read pointer being the RdPtr pointer, and does not provide support for read pointer to mean the ShfPtr pointer [FIG. 4].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomsen et al. (US 5,278,956) in view of Yasoshima (US 2002/0078317).

8. As per claims 15, Thomsen discloses an apparatus - hence a high performance buffering technique for use with a serial peripheral interface [FIG. 4; col. 6, ll. 3-19] to facilitate high data rates, said buffering technique comprising the steps of:

initializing a transmitter FIFO [18, FIG. 4] by writing data to a data register [writing data to location designated by write pointer of transmitter FIFO; col. 2, l. 66-col. 3, l. 23];

performing a transmit buffering sequence to prepare for the transmitting of the data [incrementing a write pointer of the transmitter FIFO and incrementing a counter representing the number of bytes in the transmitter FIFO [col. 2, l. 66-col. 3, l. 23]];

performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time [reading data from a location in the transmitter FIFO designated by a read pointer of the transmitter FIFO; writing the data to a transmit shift register [20, FIG. 4]; shifting of the transmit shift register [to communication station 17, FIG. 4]; and receiving and storing new data in a receive shift register [16, FIG. 4] in a location of a receiver FIFO [12, FIG. 4] designated by a write pointer of the receiver FIFO [FIG. 4; col. 2, l. 66-col. 3, l. 23; col. 6, ll. 3-19] - the architecture of FIG. 4 with transmitter and receiver shift registers and transmitter and receiver FIFOs allows full duplex communication, hence facilitates transmitting of data from transmitter FIFO and receiving of new data by the receiver FIFO at substantially the same time]; and

performing a receive buffering sequence to prepare for the receipt of additional new data [incrementing a write pointer of the receiver FIFO to identify a new location for receiving data; and incrementing a counter to indicate that new data has been received [col. 2, l. 66-col. 3, l. 23]].

Thomsen, therefore, discloses the invention except for the transceiver FIFO and the receiver FIFO being arranged within a single buffer.

Yasoshima discloses arranging multiple FIFOs within a single buffer to accommodate applications processing distinct data segments and maximize the utilization of memory [[0006], ll. 1-4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the transceiver FIFO and the receiver FIFO within a single buffer, as is taught by Yasoshima, because such arrangement would accommodate applications processing distinct data segments (as data transmitted by the CPU and data read by the CPU represent distinct data segments) and maximize the utilization of memory.

9. As per claims 16-17, Thomsen discloses writing the data into a location of said buffer as designated by a write pointer [col. 2, l. 66-col. 3, l. 23]; and incrementing a write pointer to prevent a next byte to be transmitted from overwriting a previous written byte; and incrementing a write shift counter to facilitate tracking of a number of bytes available for transmission [col. 2, l. 66-col. 3, l. 23].

10. As per claims 18-19, Thomsen discloses reading the data from a location in the buffer designated by a read pointer of transmitter FIFO (i.e. a shift pointer - as explained

below); writing the data to a transmit shift register; shifting of the transmit shift register; and receiving and storing the new data in a receive shift register in a location of said buffer designated by a write pointer of the receiver FIFO (i.e. a read pointer of the transmitter FIFO or the shift pointer - as explained below); incrementing a write pointer of receiver FIFO (i.e. a shift pointer - as explained below) to identify a new location in the buffer for receiving data; and incrementing a counter to indicate that the new data has been received [col. 2, l. 66-col. 3, l. 23]. Yasoshima discloses the read pointer of the transmitter FIFO functioning as a boundary for the receiver FIFO [FIG. 2(b); [0009]], hence a shift pointer (as the read pointer of the transmitter FIFO and the write pointer of the receiver FIFO will be at the same location after shifting of the shift registers).

11. As per claim 20, the combination of Thomsen and Yasoshima does not teach interrupting a CPU if the data is ready for transmitting and said buffer is approximately full, and interrupting the CPU if said buffer is ready to receive data and said buffer is approximately empty. Since it was known in the art the time the invention was made to interrupt a CPU when data is ready for transmitting and the buffer is approximately full to prevent buffer overflow, and to interrupt the CPU when the buffer is ready to receive data and the buffer is approximately empty to prevent buffer underflow, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate such interruptions in order to prevent buffer overflow or buffer underflow.

12. As per claim 21, Thomsen in combination with Yasoshima above, discloses a high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of:

indicating a location in a single buffer where a CPU can write data to be transmitted [write pointer of transmitter FIFO];

indicating a location in said single buffer where any received data can be stored for reading by the CPU [read pointer of receiver FIFO];

indicating a location where data to be transmitted is located [read pointer of transmitter FIFO, or shift pointer] and a location where the received data will be stored [write pointer of receiver FIFO, or shift pointer] after shifting of any registers is completed [after shifting the transmitter shift register and the receiver shift register];

tracking a number of bytes of data that need to be transmitted [counter indicating data level in transmitter FIFO]; and

tracking a number of bytes of data that have been received [counter indicating data level in receiver FIFO].

Response to Arguments

13. Applicant's arguments with respect to claims 15-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kim Huynh, can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

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Effective December 1, 2003, hand-carried patent application related incoming correspondences would be to a centralized location.

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01/06/2006

TQN
January 6, 2006